30V N-Ch Power MOSFET

V_{DS}	30	V
	3.9	m
	V_{GS}=4.5V	

Part Number	Package	Marking
HTS050N03	SOIC-8	TS050N03

Parameter	Symbol	Conditions	Value	
Continuous Drain Current (Silicon Limited)	I_D	T_A=25	20	A
		T_A=100	13	
Drain to Source Voltage	V_{DS}	-	30	V
Gate to Source Voltage	V_{GS}	-	±20	V

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.5	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=20V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=24V, T_j=125	-	-	25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	3.9	5	mΩ
		V_{GS}=4.5V, I_D=15A	-	7.1	9	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	28	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.3	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	-	2935	-	pF
Output Capacitance	C_{oss}		-	217	-	
Reverse Transfer Capacitance	C_{rss}		-	142	-	
Total Gate Charge (10V)	Q_g(10V)	V_{DD}=15V, I_D=20A, V_{GS}=10V	-	52	-	nC
Total Gate Charge (4.5V)	Q_g(4.5V)			32		
Gate to Source Charge	Q_{gs}		-	5.7	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	7.2	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_G=2.7Ω,	-	25	-	ns
Rise time	t_r		-	20	-	
Turn off Delay Time	$t_{d(off)}$		-	70	-	
Fall Time	t_f		-	20	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=10A	-		1.2	V
Reverse Recovery Time	t_{rr}	I_F=10A, dI_F/dt=100A/μs	-	35	-	ns
Reverse Recovery Charge	Q_{rr}		-	15	-	nC

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

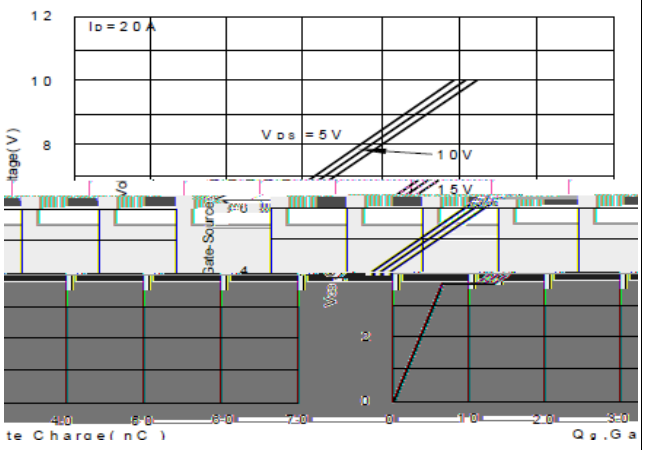


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

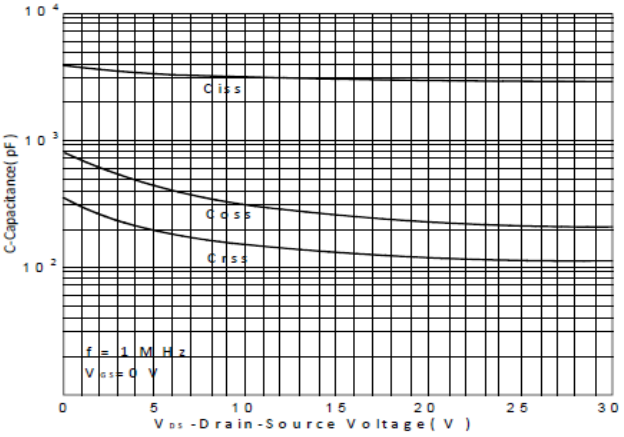


Figure 9. Maximum Safe Operating Area

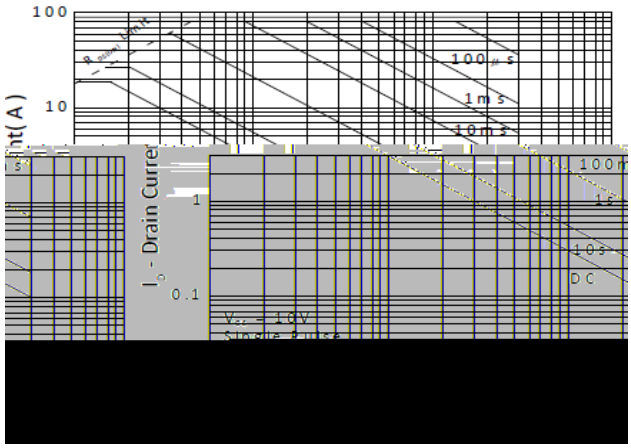


Figure 10. Single Pulse Maximum Power Dissipation

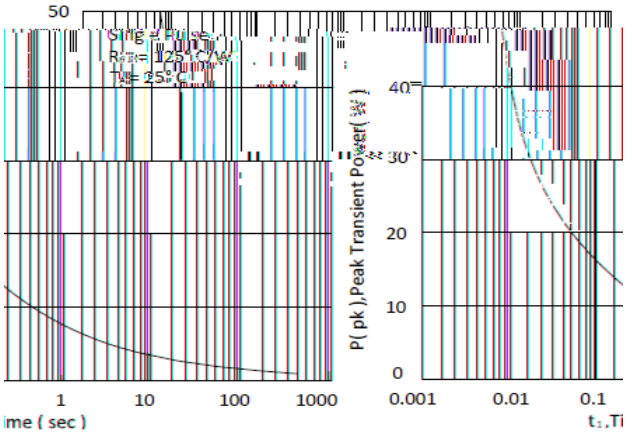
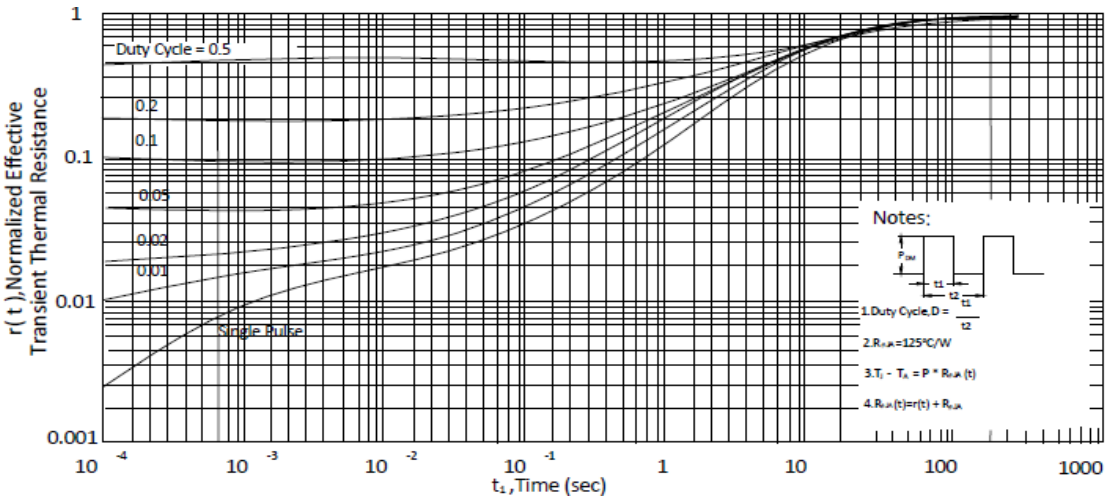
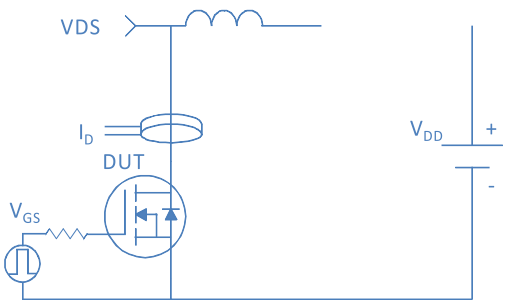


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

SOIC-8, 8 leads